```
     INDEX 'WPIX, JAPIO, PATOSWO, PATOSEP' ENTERED AT 15:16:15 ON 03 SEP 2004
SET ABB=ON  PLU=ON
L1              QUE GATE#(A)(DOUBLE OR DUAL OR FIRST OR SECOND
                OR TOP OR BOTTOM OR TWO OR TWIN)
L2              QUE BOX OR BURIED(A) OXIDE#
L3              QUE BREAKDOWN(W)(V OR VOLT#### OR POTN OR POTEN?) OR SPECIFIC(W)
                  ON(W)(RESISTIV? OR RESIST!NCE? OR CONDUCTIVIT?)
L4              QUE 7440-21-3 OR SI OR SILICON OR POLYSI
L5              QUE (ZONE# OR REGION# OR AREA# OR SEGMENT? OR SUBDIV? OR DIVISION? OR
                  DIVIDED OR COMPARTMENT? OR PART# OR PORTION#)
L6              QUE DRIFT(2A) L5
L7              QUE BODY(2A) L5
L8              QUE SOURCE(2A) L5
L9              QUE L1 AND L2 AND L3 AND L4 AND L5 AND L6 AND L7 AND L8
L10             QUE L1 AND L2 AND L3 AND L5 AND L6 AND L7 AND L8
L11             QUE L1 AND L2 AND L3 AND L6
L12             QUE L1 AND L2 AND L3
L13             QUE L12 NOT WO 2003050884/PN

     INDEX 'WPIX, EUROPATFULL, PCTFULL, FRFULL, JAPIO, PATDPAFULL, PATOSEP,
     HCAPLUS' ENTERED AT 15:50:02 ON 03 SEP 2004
L14             QUE L13

     FILE 'PCTFULL, EUROPATFULL, WPIX' ENTERED AT 15:59:10 ON 03 SEP 2004
L15          39 S L14
L16          37 S L15 AND (L4 OR (L6 OR L7 OR L8))

     INDEX 'HCAPLUS, INSPEC, COMPENDEX, SCISEARCH, PASCAL, ELCOM, ENERGY,
     AEROSPACE, DISSABS, METADEX, ANTE, NTIS, CEABA-VTB, CONFSCI, EMA, ENTEC,
     FEDRIP, RDISCLOSURE, SIGLE' ENTERED AT 16:21:11 ON 03 SEP 2004
L17             QUE L16
L18             QUE L1 AND L2 AND L3
L19             QUE L18 NOT WO 2003050884/PN

     FILE 'SCISEARCH, DISSABS' ENTERED AT 16:42:34 ON 03 SEP 2004
L20           2 S L19

     FILE 'WPIX, PCTFULL, EUROPATFULL' ENTERED AT 16:44:30 ON 03 SEP 2004
L21          37 DUP REM L16 (0 DUPLICATES REMOVED)
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☐ **L21 ANSWER 37 OF 37 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-455712 [43] WPIX Full Text

Title

N-type metal oxide semiconductor trigger silicon controlled rectifier in silicon -on-insulator has doping regions in N-type well and in P-type well, gate in P-type well, and dummy gate in N-type well.

Author/Inventor

HONG, G; KE, M; TANG, T; HUNG, K; KER, M

Patent Assignee/Corporate Source

(LIAN-N) LIANHUA ELECTRONICS CO LTD; (UNMI-N) UNITED MICROELECTRONICS CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6521952	B1	20030218	(200343)		28	H01L023-62
CN 1414639	A	20030430	(200351)			H01L029-74

Application Details

US 6521952 B1 **US** 2001-682811 **20011022;**

Abstract

US 6521952 B UPAB: 20030707

NOVELTY - An N-type metal oxide semiconductor (NMOS) trigger ***silicon*** controlled rectifier in ***silicon*** -on-insulator (SOI-NSCR) has a P-type well and an N-type well in SOI substrate; first P+ and N+ doping regions in N-type well for use as anode; second P+ and N+ doping regions in P-type well for use as cathode; third N+ doping region across wells; gate in P-type well; and dummy gate in N-type well.

DETAILED DESCRIPTION - An N-type metal oxide semiconductor (NMOS) trigger ***silicon*** controlled rectifier in ***silicon*** -on-insulator (SOI-NSCR) comprises a P-type well (104) and an N-type well (106) in a single crystal ***silicon*** layer on a surface of a ***silicon*** -on-insulator substrate (101); a first P+ doping region (108) and a first N+ doping region (110) in the N-type well for use as an anode of the SOI-NSCR; a second P+ doping region (116) and a second N+ doping region (114) in the P-type well for use as a cathode of the SOI-NSCR, wherein the first P+ doping region, N-type well, P-type well and second N+ doping region form a lateral ***silicon*** controlled rectifier (SCR); a third N+ doping region (112) across the N-type well and the P-type well; a gate (122) in the P-type well and the third N+ doping region, wherein the gate and the second N+ doping region form an NMOS (123); and a dummy gate (124) in the N-type well for isolating the first P+ doping region and the third N+ doping region.

An INDEPENDENT CLAIM is also included for an electrostatic discharge (ESD) protection circuit adapted to electrically connect to an input/output (I/O) pad, a Vss power terminal and a Vdd power terminal comprising an NMOS-trigger ***silicon*** controlled rectifier in ***silicon*** -on-insulator having an anode electrically connected to the I/O pad and a cathode electrically connected to the Vss power terminal; a PMOS-trigger ***silicon*** controlled rectifier in ***silicon*** -on-insulator (SOI-PSCR) having an anode electrically connected to the Vdd power terminal and a cathode electrically connected to the I/O pad; a first diode having an anode electrically connected to the Vss power terminal and a cathode electrically connected to the I/O pad; a second diode having an anode electrically connected to the I/O pad and a cathode electrically connected to the Vdd power terminal; a first resistor electrically connecting the I/O pad to a first dummy gate of the SOI-NSCR and a second resistor electrically connecting the Vss power terminal to a ***first gate*** of the SOI-NSCR; and a third resistor electrically connecting the I/O pad to the second dummy gate of the SOI-PSCR and a fourth resistor electrically connecting the Vdd power terminal to the ***second gate*** of the SOI-PSCR.

USE - For an on-chip ESD protection circuit (claimed).
ADVANTAGE - Provides an SCR with a compact structure and achieves a quick turn-on speed for ESD protection circuit.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic diagram of an SOI-NSCR device structure in a partially depleted SOI CMOS process.
Silicon -on-insulator substrate 101
P-type substrate 102
P-type well 104
N-type well 106
First P+ doping region 108
First N+ doping region 110
Third N+ doping region 112
Second N+ doping region 114
Second P+ doping region 116
Gate insulator 118
Gate material 120
Gate 122
NMOS 123
Dummy gate 124
Shallow trench isolation areas 126
Buried oxide layer 128 Dwg.5a/11

Technology

US 6521952 B1 UPTX: 20030707 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: When a positive transient voltage is applied across the anode and the cathode of the SOI-NSCR, the positive transient voltage generates a current flowing from the first P+ doping region to the N-type well. When the positive transient voltage is greater than a junction ***breakdown voltage***, the junction breaks down so that the current incurred from the positive transient voltage flows across the junction and is discharged to the cathode through the second N+ doping region. When a voltage is applied to the gate of the NMOS that turns on the NMOS, a forward bias is created that causes the SOI-NSCR to turn on, and current incurred from a positive transient voltage across the anode and the cathode is discharged to the cathode across a junction of the P-type well and the third N+ doping region. The third N+ doping region is used as an N trigger node. A voltage applied to the third N+ doping region generates a trigger current through the N trigger node to cause the lateral SCR to enter a latch state and to quickly trigger on the SOI-NSCR and current incurred from a positive transient voltage across the anode and the cathode is discharged to the cathode across a junction of the P-type well and the third N+ doping region. When a negative transient voltage is applied across the anode and the cathode of the SOI-NSCR, the negative transient voltage generates a current flowing from the second P+ doping region to the P-type well and a junction of the P-type well and the N-type well is forward biased so that the current incurred from the negative transient voltage flows from the N-type well to the anode through the first N+ doping region. The junction of the third N+ doping region and the P-type well is utilized for reducing the trigger voltage for the SOI-NSCR device. The junction ***breakdown voltage*** for the P-type well and the third N+ doping region is lower than the junction ***breakdown voltage*** for the P-type well and the N-type well. The SOI-NSCR further comprises spacer(s) surrounding each gate and a lightly doped drain (LDD) underneath each spacer. The first P+ doping region, second P+ doping region, first N+ doping region and the second N+ doping region are not in contact with the isolator in the SOI substrate so that the SOI-NSCR is capable of integration in a partially depleted or a fully depleted SOI CMOS process.

☐ **L21 ANSWER 5 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number

2002037200

Title

VOLTAGE SUPPLY CIRCUIT

Patent Information

WO 2002037200 A1 20020510

PATENT-FAMILY:

PUB-NO PUB-DATE

WO 200237200 A1 May 10, 2002
US 20020113653 A1 August 22, 2002
APPLICATION-DATA:
US20020113653A1 N/A 2001US-0040060 **October 29, 2001**

Abstract

A circuit comprises a first JFET (21) connected in series to a second JFET (22) wherein a gate (26) of the first JFET (21) is connected to a source of the second JFET (22) and is connected to a load (30) and is not connected to ground. The gate of the second JFET (22) is connected to ground. The JFETs are preferably formed by ***silicon*** on insulator integration technology.

DETD . . . situation is obtained by means of the equal oxide thicknesses, which is favorable for the electric field distribution and thus for the **breakdown voltage** of the transistor. A further improvement may be obtained in that the **drift region** 318 is provided with a profiled doping whose concentration increases linearly in the direction from the source to the drain.

So, the JFET transistor preferably used in the present invention is a deep depletion MOS transistor provided in a thin **silicon** layer 305 adjoining a surface 304 of a **silicon** body 303 and isolated from a **silicon** substrate 307 by a **buried oxide** layer 306. The channel region 313 of a first conductivity type is provided with at least one and preferably a plurality of. . . 313. This enables the transistor to be operative also at high voltages havi ng values at which the substrate 307 and the **buried oxide** layer 306 are operative respectively as a **second gate** on a **second gate** dielectric.

☐ **L21 ANSWER 6 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number
2002025700

Title
SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE

Patent Information
WO 2002025700 A2 20020328

Priority number(s): US20000234219P 20000921

Abstract

A power semiconductor device (10) has an active region that includes a ***drift region*** (20). At least a ***portion*** of the ***drift region*** (20) is provided in a membrane)16) which has opposed top and bottom surfaces (15, 17). In one embodiment, the top surface (15) of the membrane (16) has electrical terminals connected directly or indirectly thereto to allow a voltage to be applied laterally across the ***drift region*** (20). In another embodiment, at least one electrical terminal is connected directly or indirectly to the top surface (15) and at least one electrical terminal is connected directly or indirectly to the bottom surface (17) to allow a voltage to be applied vertically across the ***drift region*** (20). In each of these embodiments, the bottom surface (17) of the membrane (16) does not have a semiconductor substrate positioned adjacent thereto.

. . .

for example a diode, a transistor, a thyristor, a MOS controllable device such as a MOSFET, an insulated gate bipolar transistor (IGBT), a **double gate** device, etc.

In the preferred embodiments discussed further below, there is provided a high voltage, power device with high **breakdown voltage** capacity coupled with excellent isolation and reduced self-heating.

The arrangement may be such that only **part** of the **drift region** is provided in the membrane.

In the first and second aspects, where only a **part** of the **drift region** is provided in the membrane, preferably the high voltage terminal end of the **drift region** is contained within the membrane; the remainder of the **drift region**, including the low voltage terminal end, may remain outside the membrane.

☐ **L21 ANSWER 7 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number
2002015277

Title
DENSE ARRAYS AND CHARGE STORAGE DEVICES, AND METHODS FOR MAKING SAME

Patent Information
WO 2002015277 A2 20020221

Priority number(s): **US**20000639579 **20000814**; US20000639702 20000814; US20000639749 20000817; US20000745125 20001221; US20010801233 20010306; US20010279855P 20010328

Abstract
There is provided a monolithic three dimensional array of charge storage devices which includes a plurality of device levels, wherein at least one surface between two successive device levels is planarized by chemical mechanical polishing.

DETD
. . .
as shown in Figure 41. The width of the gate contact via 4029 is substantially the same as the width of the **first gate** electrode 4009 because the via sidewalls are the inner sidewalls of the sidewall spacers 4021. Therefore, the gate contact vias 4029 are. . .

A **second gate** electrode conductive material 4031 is then deposited over the entire device, as shown in Figure 42.- Preferably, the material 4031 comprises a. . . as 200 nm thick. The silicide layer 4035 is preferably 50 to 100 nm thick, such as 60 nm thick. Alternatively, the **second gate** material can also be formed from a single layer of silicide, metal, or any other combination of heavily doped amorphous or polycrystalline-**silicon**, silicide, and metal that makes a good ohmic.contact with the **first gate** electrodes 4009.

☐ **L21 ANSWER 8 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number
2001047030

Title
DEPLETION TYPE MOS TRANSISTOR

Patent Information
WO 2001047030 A1 20010628

Abstract
The invention relates to a SOI deep depletion MOS transistor provided in a thin ***silicon*** layer (5) adjoining a surface (4) of a ***silicon*** body (3) and insulated from a ***silicon*** substrate (7) by a ***buried oxide*** layer (6). The channel region (13) of a first conductivity type is provided with at least one and preferably a plurality of zones (16) of the opposite conductivity type adjoining the surface to remove minority carriers from the interface between the channel and the gate oxide (15). The zones (16) extend across the whole thickness of the channel and adjoin the ***buried oxide*** at the side of the channel remote from the gate dielectric. Due to this construction, minority carriers are removed also from the rear side of the channel. This enables the transistor to be operative also at high voltages having values at which the substrate and the ***buried oxide*** operate as a ***second gate*** and as a ***second gate*** dielectric, respectively. The transistor may be used to advantage in high-voltage ICs comprising a low-voltage circuit part operated with a low supply voltage generated by the transistor.

. . .

Preferably, a field plate is provided above the **drift region**, which renders possible, as is known, a better combination of a high **breakdown voltage** (for example with the resurf effect) and a low on-resistance. A further embodiment, in which a more or less symmetrical field distribution is obtained, is characterized in that the distance between the field plate and the **drift region** is equal or at least substantially equal to the distance between the **drift region** and the semiconductor substrate.

☐ **L21 ANSWER 9 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number
2001018876

Title
BIPOLAR MOSFET DEVICE

Patent Information
WO 2001018876 A1 20010315

Abstract
There is disclosed a semiconductor device comprising: at least one cell comprising a base region (32) of a first conductivity type having disposed therein at least one emitter region (36a, 36b) of a second conductivity type; a first well region (22) of a second conductivity type; a second well region (2a) of a first conductivity type; a ***drift region*** (24) of a second conductivity type; a collector region (14) of a first conductivity type; a collector contact (16) in which each cell is disposed within the first well region (22) and the first well region (22) is disposed within the second well region (20); the device further comprising: a ***first gate*** (61) disposed over a base region (32) so that a MOSFET channel can be formed between an emitter region (36a, 36b) and the first well region (22); the device further comprising: a ***second gate***

disposed over the second well region (20) so that a MOSFET channel can be formed between the first well region (22) and the ***drift region*** (24).
. . . first well region (22) of a second conductivity type; a second well region (2a) of a first conductivity type; a ***drift region*** (24) of a second conductivity type; a collector region (14) of a first conductivity type; a collector contact (16) in. . . (22) and the first well region (22) is disposed within the second well region (20); the device further comprising: a ***first gate*** (61) disposed over a base region (32) so that a MOSFET channel can be formed between an emitter region (36a, 36b) and the first well region (22); the device further comprising: a ***second gate*** disposed over the second well region (20) so that a MOSFET channel can be formed between the first well region (22) and the ***drift region*** (24).

☐ **L21 ANSWER 11 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number

2000038240

Title

FLOATING GATE MEMORY CELL STRUCTURE WITH PROGRAMMING MECHANISM OUTSIDE THE READ PATH

Patent Information

WO 2000038240 A1 20000629

Abstract

A non-volatile memory cell structure includes a floating gate, a reverse breakdown hot carrier injection element and a sense transistor. The reverse breakdown hot carrier injection element is at least partially formed in a first region of a semiconductor substrate under at least a portion of the floating gate. The sense transistor is at least partially formed in a second region of a semiconductor substrate, isolated from the first region, and under at least a portion of the floating gate. A read transistor may be connected to the sense transistor. In one embodiment, the read transistor is at least partially formed in the second region of a semiconductor substrate, and connected to the sense transistor.

DETD . . .
of the programming voltage below current known levels.

In the devices shown in Figures 11 - 12, separate program and erase path are utilized, hence a **source region** is for example connected to a write enable line (WBL,) while the **source region** is connected to the program enable line (WBLP). It should be recognized that the separate program and erase paths shown in. . .

Element 1240 includes a drain region 1242 coupled to a first program line (WBL). and a **source region** 1244, and floating gate (FG) at region 1246. Nonvolatile floating gate transistor 15 includes a source 1232 and drain 1236, and floating. . .

CLMEN 7 The structure as defined in claim 6 wherein a **first gate** oxide overlies said first channel region and a **second gate** oxide overlies said second channel region and a third gate oxide overlies said third channel region.
17
. The structure as defined in claim 7 wherein the first and

☐ **L21 ANSWER 13 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number
2000038227

Title
METHOD OF MAKING A SEMICONDUCTOR DEVICE INCLUDING AN ASYMMETRICAL FIELD-EFFECT TRANSISTOR

Patent Information
WO 2000038227 A1 20000629

Abstract
A method of making a semiconductor device including an asymmetric field-effect transistor (100), comprising the steps of forming a dielectric structure (1404) over a first portion of a substrate comprising a first lightly doped drain region (1300), forming sidewall spacers adjacent said dielectric structure over a second portion of said substrate, forming an insulating layer (1601) adjoining said spacers over said second portion, selectively removing the spacers to form a gate oxide (1703) at their location, depositing a first layer comprising ***Si*** (1704), etching portions of said first layer and gate oxide to expose a part of said second substrate portion, depositing a second layer comprising ***Si*** (1801) over the resulting structure, etching said first and second layers comprising ***Si*** to form separate source (1904), ***first gate*** (1902), ***second gate*** (1903), and drain (1901) electrodes. A bipolar transistor (120) may be included in the semiconductor device and formed simultaneously with the field-effect transistor.

DETD . . . being reduced. However, this reduction in size degrades many output characteristics of the MOSIFETs. For example, MOSFETs with submicron dimensions have lower **breakdown voltage** and decreased output impedance because of modulation of the channel length due to the drain-induced barrier lowering. These disadvantages severely limit the. . .

Accordingly, a need exists for a semiconductor component having transistors with sufficiently high **breakdown voltage** , output impedance, and frequency response. A need also exists for a.method of manufacturing the semiconductor component that does not substantially increase the. . .

☐ **L21 ANSWER 14 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number
2000031793

Title

PERIPHERAL TRANSISTOR OF A NON-VOLATILE MEMORY

Patent Information

WO 2000031793 A1 20000602

Abstract

In a non-volatile memory comprising a region (2) for core memory cells and a peripheral region
(4a) on a substrate (6), a method for improving the electrostatic discharge (ESD) robustness of the non-volatile memory comprises the steps of lightly doping the ***source region*** (18) and the drain region (20) of a peripheral transistor (12) in the peripheral region (4a) with a first n-type dopant, providing a double diffusion implant mask (10) having an opening over the region (2) for the
core memory cells and also an opening (8) over the peripheral region (4a), and performing a double
diffusion implantation through the opening (8) over the peripheral region (4a). In an embodiment,
the step of performing the double-diffusion implantation comprises the steps of implanting a second
n-type dopant comprising phosphorus into the ***source*** and drain ***regions*** (18) and (20), and implanting a third n-type dopant comprising arsenic into the ***source*** and drain ***regions*** (18) and (20) subsequent to the step of implanting the second n-type dopant.

DETD . . .

is that it is able to offer a high level of ESD protection without producing a high leakage current at a low **breakdown voltage**. Yet a further advantage of the
present invention is that both the peripheral transistors and the core memory cells
are subjected to. . .

. . .

is a sectional view, taken along the sectional line I 0 1 a- I 0 1 b of FIG. 2, of **source** and drain **regions** of a transistor
in the peripheral region before
a spacer oxide is provided around the gate;
4
FIG. 4 is a sectional view. . . provided; and
FIG. 5 is a sectional view of the transistor of FIG. 4, showing a lateral
current flow from the drain **region** to the **source region**.

. . .

memory cells is an area of substrate 6 provided for the
implementation of an array of memory cells, usually with a **dual -gate** structure
comprising first and second polysilicon layers (POLY-I and POLY-2). The peripheral regions 4a, 4b, 4c.... 4h are provided on the substrate. . .

☐ **L21 ANSWER 16 OF 37 PCTFULL COPYRIGHT 2004 Univentio on STN**

Accession Number

1999046809

Title

DEVICES FORMABLE BY LOW TEMPERATURE DIRECT BONDING

Patent Information

WO 9946809 A1 19990916

Abstract

A semiconductor device includes a laterally extending semiconductor base (82, 96), a buffer
(83) adjacent the base and having a first conductivity type dopant, and a laterally extending
emitter (85) adjacent the buffer and opposite the base and having a second conductivity type dopant.
The buffer (83) is thin and has a fist conductivity type dopant concentration greater than a second conductivity type dopant concentration in adjacent emitter portions to provide a negative
temperature coefficient for current gain and a positive temperature coefficient for forward voltage
for the device. The buffer may be ***silicon*** or germanium. A low temperature bonded interface (103) may be between the emitter and the buffer or the buffer and the base. Another embodiment of a device may include a laterally extending localized lifetime killing portion (92, 102) between oppositely doped first and second laterally extending portions. The localized lifetime killing portion may comprise a
plurality of laterally confined and laterally space apart lifetime killing regions. Another device
may include one or more PN junctions.

DETD . . .
shown in FIG. 3, various dopant regions are formed in the upper surface of the substrate 80, along with the illustrated **second gate** region 81. The illustrated processed portion
further includes an N-type base 82, an N-type buffer layer 83 on the N-type base,. . .
. . .
N-type base 96, a P-type base 97 on the N-type base, an N+ emitter 98 on the N-type base, a **first gate**
99, a cathode laver 100, and the illustrated P+ region 101. The second substrate 95 also illustratively includes the lifetime killing implants. . .
. . .

The experimental measurements show that low temperature direct wafer bonding is a
suitable approach for fabricating **double-gate** MOSFET
controlled switching power devices. Near
ideal electrical conduction across the bonding interface can be obtained for bond anneal
temperatures in the. . .
. . .
If the P+ substrate concentration is too high (such that a P+ to N+ junction would have too low of a **breakdown voltage**, have too much leakage current, or be too high concentration
so that it is difficult to have an N+ buffer concentration. . .

☐ **L21 ANSWER 20 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP 1298721 EUROPATFULL ED 20030408 EW 200314 FS OS
US2003068844 (A1)

Priority number(s): US20010964472 **20010928**

Title

Method of making high-voltage bipolar/CMOS/DMOS (BCD) devices.

Abstract

A process for making an integrated circuit is described wherein sequence of mask steps is applied to a substrate or epitaxial layer of p-type material. The sequence consists of the following steps:
(1) applying a first mask and forming at least one N-well in said p-type material therethrough;
(2) applying a second mask and forming an active region therethrough;
(3) applying a third mask and forming a p-type field region therethrough;
(4) applying a fourth mask and forming a gate oxide therethrough;
(5) applying a fifth mask and carrying out a p-type implantation therethrough;
(6) applying a sixth mask and forming polysilicon gate regions therethrough;
(7) applying a seventh mask and forming a p-base region therethrough;
(8) applying an eighth mask and forming a N-extended region therethrough;
(9) applying a ninth mask and forming a p-top region therethrough;
(10) applying a tenth mask and carrying out an N+ implant therethrough;
(11) applying an eleventh mask and carrying out a P+ implant therethrough;
(12) applying a twelfth mask and forming contacts therethrough;
(13) applying a thirteenth mask and depositing a metal layer therethrough;
(14) applying a fourteenth mask and forming vias therethrough;
(15) applying a fifteenth mask and depositing a metal layer therethrough; and
(16) applying a sixteenth mask and forming a passivation layer therethrough. Up to any three of mask steps 4, 7, 8, and 9 may be omitted depending on the type of integrated circuit.

DETDEN . . .
Each mask step is associated with the sub-processes identified in the table. For example, in step 1, starting from bulk P-type **silicon** , an initial oxidation takes place followed by photolithography to define the mask. An N-type implant takes place to form the. . . Figure . . . the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide) so as to produce a **Dual gate** oxide basic thirteen-mask CMOS process. As shown in Figure 2 and Figure 10, this **Dual gate** oxide basic thirteen-mask CMOS process allows the integration of another standard N-MOSFET with high-voltage gate oxide, of another standard P-MOSFET. . .

Again, . . . with very different operating voltage characteristics. They are also associated with a wide variety of other electrical performances such as **breakdown voltage**, cut-off frequency, specific channel resistance, size figure-of-merit, which allows the designer to cherry-pick the ideal combination of active components for. . .
The . . . which would otherwise be achieved using independent substrates and/or much more complex processes. The invention can be practiced on a **Silicon** Over Isolator (SOI) substrate and achieve higher **breakdown voltage** up to about 1200 volts for the following active components if the **silicon** layer over the **buried oxide** is thicker then 1.5 μm: a high-voltage double extended N-LDMOSFET shown in Figure 32a; a high-voltage double extended N-LDMOSFET shown. . .

☐ **L21 ANSWER 21 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**
Accession Number
EP854519 EUROPATFULL ED 19980802 EW 199830 FS OS
Title
SOI MOS field effect transistor.

Abstract

A SOI MOS field effect transistor includes: a superficial top semiconductor layer of a first conductivity type formed on a SOI substrate; ***source*** and drain ***regions*** of a second conductivity type arranged apart from each other on the top semiconductor layer; a P-type first channel region, an N.sup+.-type floating region, and a P-type second channel region formed in this order in a self-aligned manner and disposed between the N.sup+.-type ***source region*** and the N.sup+.-type drain region for an N-type MOSFET, or an N-type first channel region, a P.sup+.-type floating region, and an N-type second channel region formed in this order in a self-aligned manner and disposed between the P.sup+.-type ***source region*** and the P.sup+.-type drain region for a P-type MOSFET; and ***two gate*** electrodes for controlling the first and second channel regions, wherein a doping concentration of the second channel region adjacent to the drain region is lower than a doping concentration of the first channel region adjacent to the ***source region***. <image>

☐ **L21 ANSWER 22 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP789144 EUROPATFULL ED 19970824 EW 199733 FS OS

Title

A turbine engine ignition exciter circuit incluiding low voltage lockout control.

Abstract

The invention provides an improved turbine engine ignition exciter circuit. Energy stored in an exciter tank capacitor is subsequently switched to the load (igniter plug) through a novel thyristor switching device specifically designed for pulse power applications. The switching device is designed and constructed to include, for example, a highly interdigitated cathode/gate structure. The semiconductor switching device is periodically activated by a trigger circuit which may be comprised of either electromagnetic or optoelectronic triggering circuitry to initiate discharge of energy stored in exciter tank capacitor to mating ignition lead and igniter plug. Likewise, the present invention allows new flexibility in the output PFN (Pulse Forming Network) stage, eliminating need for specialized protective output devices such as saturable output inductors. Due to considerably higher di/dt performance of the device, true high voltage output pulse networks may be utilized without damage to the semiconductor switching device. An exemplary embodiment of invention contains a novel feedback network which causes thyristor timing (trigger) and DC-DC converter circuits to compensate for varying igniter plug wear and dynamic engine combustor conditions, tailoring exciter spark rate, output voltage and energy to account for dynamic load conditions. <image>

DETDEN Likewise, . . . significant improvement over conventional single thyristor exciters since it is specifically designed for pulse discharge applications. For example, the nominal (**breakdown**) **voltage** rating of PPT devices according to exemplary embodiments is greater than, for example, 5 kV. Consequently, despite high (for example,. . .

The . . . of the PPT cathode carrier concentration profile of Fig. 12;

FIG. 14 provides a summary of an exemplary PPT (**silicon**) manufacturing process according to the present invention;

FIG. 15 illustrates (in sheet rho versus etch time) an exemplary process. . .

The . . . virtue of its unique design and construction, is capable of driving a variety of output pulse forming networks. The unique "

double gate" PPT thyristor schematic symbol seen in block 6 of Figure 1 is used to differentiate the PPT device from conventional thyristor devices. **Double gate** leads denote the considerable interdigitation of gate and cathode structures and associated high (di/dt) current carrying capability of exemplary embodiments. . .

☐ **L21 ANSWER 26 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP749165 EUROPATFULL ED 19970307 EW 199651 FS OS

Title

Thin film transistor in insulated semiconductor substrate and manufacturing method thereof.

Abstract

It is an object to obtain a semiconductor device with the LDD structure having both operational stability and high speed and a manufacturing method thereof. A high concentration region (11) with boron of about 1+10.sup18./cm.sup3. introduced therein is formed extending from under a channel formation region (4) to under a drain region (6) and a ***source region*** (6') in a ***silicon*** substrate (1). The high concentration region (11) is formed in the surface of the ***silicon*** substrate (1) under the channel formation region (4), and is formed at a predetermined depth from the surface of the ***silicon*** substrate (1) under the drain region (6) and the ***source region*** (6'). A low concentration region (10) is formed in the surface of the ***silicon*** substrate (1) under the drain region (6) and the ***source region*** (6'). The formation of the high concentration region only in the surface of the semiconductor substrate under the channel formation region surely suppresses an increase in the leakage current and an increase in the drain capacitance. <image>

DETDEN

JP . . . is formed in a semiconductor substrate under a channel in such a way that it is not in contact with **source regions** and drain regions. That is to say, the high-concentration impurity diffusion region, for punchthrough prevention use, whose conductivity type is the same as that of the semiconductor substrate is arranged in an intermediate position between the **source regions** and the drain regions in the substrate under the channel. Thereby, it is possible to reduce a punchthrough current between. . .

According . . . layer formed on the first insulating layer, the first semiconductor layer including a region of the second conductivity type, a **first gate** insulating film selectively formed on the first semiconductor layer, a **first gate** electrode formed on the **first gate** insulating film, and first and second sidewalls formed on sides of the **first gate** electrode, respectively, wherein the first semiconductor layer is defined as a first channel formation region under the **first gate** insulating film, defined as first and second additional semiconductor regions of the second conductivity type under the first and second. . . semiconductor regions respectively on sides opposite to the first channel formation region, and a predetermined voltage is applied to the **first gate** electrode to cause a current to flow between the first semiconductor region and the second semiconductor region through the channel. . . layer formed on the second insulating layer, the second semiconductor

layer including a region of the first conductivity type, a **second gate** insulating film selectively formed on the second semiconductor layer, a **second gate** electrode formed on the **second gate** insulating film, and third and fourth sidewalls formed on sides of the **second gate** electrode, respectively, wherein the second semiconductor layer is defined as a second channel formation region under the **second gate** insulating film, defined as third and fourth additional semiconductor regions of the first conductivity type under the third and fourth. . .

☐ **L21 ANSWER 27 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP836194 EUROPATFULL ED 19980503 EW 199816 FS OS
EP836194 EUROPATFULL UP 20000604 EW 200021 FS PS

Title

Semiconductor device.

Abstract

A semiconductor device including an NMOS transistor includes a first bias generating circuit 30 for generating a substrate bias VBB1 for making smaller the amount of leak current in an inactive state, a second bias generating circuit 31 for generating a substrate bias VBB2 for increasing drivability of supplying current in the active state of the NMOS transistor, and a bias selecting circuit 32 responsive to a control signal CNT for supplying the substrate bias VBB2 instead of the substrate bias VBB1 to the ***silicon*** substrate 1. By changing the potential of the substrate bias in the standby state and the active state, power consumption in the standby state can be reduced and the speed of operation in the active state can be improved. <image>

DETDEN

In . . . set to the high level, NMOS transistor 321 is turned on, and the substrate bias VBB1 is supplied to the ***silicon*** substrate 1. Meanwhile, in the active state, the control signal CNT is set to the high level, the NMOS transistor 322 is turned on, and the substrate bias VBB2 is supplied to the ***silicon*** substrate 1. By this simple structure, the substrate bias applied to the ***silicon*** substrate 1 can be changed.

The SOI-MOSFET has a MOS structure of ***silicon*** substrate 15 / ***buried oxide*** layer 14 / ***silicon*** layer 13, as viewed from the side of the ***silicon*** substrate 15. In other words, MOS structure is formed on both surfaces of the ***silicon*** layer 13. The operation when the substrate bias VBB2 (5V) is applied from the ***silicon*** substrate 15 changes dependent on whether the channel region is completely depleted or partially depleted when the voltage is applied. . . When the channel region is entirely depleted (in this example, NMOS transistor), the capacitors are coupled in series from the ***buried oxide*** film 14 to the gate dielectric thin film 4 (***buried oxide*** layer 14 / ***silicon*** layer 13 / gate dielectric thin film 4) (capacitance coupled), and the threshold voltages of the MOS transistors 11 and. . . voltages caused by the substrate bias change is the same as that of the MOS transistor formed on the bulk ***silicon*** described above. However, since the bias potential is supplied to the semiconductor layer 13 through the thick ***buried oxide*** layer 14, the change becomes smaller.

. . .

The semiconductor device differs from the semiconductor device shown in

Fig. 14 in that an NMOS ***second gate*** 18 and a PMOS ***second gate*** 19 are provided in the ***buried oxide*** film layer. The NMOS ***second gate*** 18 is provided below the ***silicon*** layer 13 of the NMOS transistor 11, and the PMOS ***second gate*** 19 is provided below the PMOS transistor 12.
Referring to Fig. 17, on the ***silicon*** layer 13, a substrate terminal 28 for receiving substrate biases VBB1 and VBB2 and a substrate terminal 29 for receiving. . .

☐ **L21 ANSWER 28 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP939439 EUROPATFULL ED 19990912 EW 199935 FS OS

Title

Method of forming fully depleted simox CMOS having electrostatic discharge protection.

Abstract

The formation of a fully-depleted, ESD protected CMOS device is described. The device is formed on an SOI or SIMOX substrate (12, 14, 16), over which an oxide pad (24) is grown to a thickness of between 10 and 30 nm. Appropriate ions are implanted into the oxide to adjust the threshold voltage of an ESD transistor (22). A portion (28) of the top ***silicon*** film (16) is thinned to a thickness no greater than 50 nm. The fully depleted CMOS devices (18) are fabricated onto the thinned top ***silicon*** film, while the ESD devices (20, 22) are fabricated onto the top ***silicon*** film (16) having the original thickness. <image> <image>

DETDEN

Buried oxide layer 14 has a thickness of between 150 nm and 300 nm. The thickness of top **silicon** layer 16 typically is between about 200 nm and 400 nm. The fabrication of three separate components that are formed. . . the wafer which contains multiple iterations of the device herein is initially prepared from a wafer of pure, single crystal **silicon**, the remains of which constitute **silicon** layer 12, and which is treated to form **buried oxide** layer 14 below top **silicon** layer 16.
A **silicon** oxide pad 24 is formed by chemical vapor deposition (CVD) to a thickness of between 10 nm and 30 nm. . .
A layer of **silicon** nitride (**SI**.sub3.N.sub4.) 26 is then deposited across the entire width of area 18, 20, 22 by CVD to a thickness of between. . .

Referring . . . of between about 1.0.dot.10.sup12. cm.sup2. and 6.0.dot.10.sup12. cm.sup-2. to adjust the threshold voltage of the n.sup-. channel transistor. For N.sup+./P.sup+. **dual gate** structures, the gate electrode of the p.sup-. channel transistor is P.sup+. doped polysilicon. Phosphorus (P) or arsenic (As) should be. . .
Moving . . . 60 keV, and an ion dose of between about 3.0.dot.10.sup15. cm.sup-2. and 10.0.dot.10.sup15. cm.sup-2.. An alternate process of an n+/p+ **dual gate** formation may also be used. The device gate areas are then covered with photoresist to allow etching of the polysilicon,. . .
Turning . . . applied to allow for source and drain ion implantation. Ion implantation results in the formation of a number of active **regions**, including a **source** 36 and a drain 38 in MOS transistor area 18; an n+ **silicon** area 40 and a p+

silicon area 42 in ESD diode area 20; and an n+ source 44 and n+ drain 46 in ESD MOST area. . . ESD MOST 22. A region 51 is located between the n.sup+. and p.sup+. regions of the diode to prevent low **breakdown voltage** and leakage current of ESD diode 20.
Thus, . . . The device is formed on an SOI or SIMOX substrate. The ESD device portion of the wafer is protected with **silicon** nitride. The top **silicon** of the fully depleted CMOS area is thinned by an oxidation process.

☐ **L21 ANSWER 34 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP564204 EUROPATFULL ED 20000423 EW 199340 FS OS STA B

Title

Semiconductor device.

Abstract

A semiconductor device including an NMOS transistor includes a first bias generating circuit 30 for generating a substrate bias VBB1 for making smaller the amount of leak current in an inactive state, a second bias generating circuit 31 for generating a substrate bias VBB2 for increasing drivability of supplying current in the active state of the NMOS transistor, and a bias selecting circuit 32 responsive to a control signal CNT for supplying the substrate bias VBB2 instead of the substrate bias VBB1 to the ***silicon*** substrate 1. By changing the potential of the substrate bias in the standby state and the active state, power consumption in the standby state can be reduced and the speed of operation in the active state can be improved.
<image>

A . . . responsive to a control signal CNT for supplying the substrate bias VBB2 instead of the substrate bias VBB1 to the ***silicon*** substrate 1. By changing the potential of the substrate bias in the standby state and the active state, power consumption. . .
DETDEN. . .

The SOI-MOSFET has a MOS structure of ***silicon*** substrate 15 / ***buried oxide*** layer 14 / ***silicon*** layer 13, as viewed from the side of the ***silicon*** substrate 15. In other words, MOS structure is formed on both surfaces of the ***silicon*** layer 13. The operation when the substrate bias VBB2 (5V) is applied from the ***silicon*** substrate 15 changes dependent on whether the channel region is completely depleted or partially depleted when the voltage is applied. . . When the channel region is entirely depleted (in this example, NMOS transistor), the capacitors are coupled in series from the ***buried oxide*** film 14 to the gate dielectric thin film 4 (***buried oxide*** layer 14 / ***silicon*** layer 13 / gate dielectric thin film 4) (capacitance coupled), and the threshold voltages of the MOS transistors 11 and. . . voltages caused by the substrate bias change is the same as that of the MOS transistor formed on the bulk ***silicon*** described above. However, since the bias potential is supplied to the semiconductor layer 13 through the thick ***buried oxide*** layer 14, the change becomes smaller.
Let . . . the PMOS transistor. The potential of the channel region which is not depleted is fixed at the potential of the ***source region*** 8. Therefore, such a capacitance coupling as occurred when it is fully depleted is not generated. Therefore, the threshold voltage. . .

The semiconductor device differs from the semiconductor device shown in Fig. 14 in that an NMOS ***second gate*** 18 and a PMOS ***second gate*** 19 are provided in the ***buried oxide*** film layer. The NMOS ***second gate*** 18 is provided below the ***silicon*** layer 13 of the NMOS transistor 11, and the PMOS ***second gate*** 19 is provided below the PMOS transistor 12.

Referring to Fig. 17, on the ***silicon*** layer 13, a substrate terminal 28 for receiving substrate biases VBB1 and VBB2 and a substrate terminal 29 for receiving. . .

In the standby state, the substrate bias VBB1 (0V) is supplied to the NMOS ***second gate*** 18 and the substrate bias VBB2 (5V) is supplied to the PMOS ***second gate*** 19 in the standby state. By the application of the substrate biases, the threshold voltage Vth of the NMOS transistor. . .

When . . . device is switched from the standby state to the active state, the substrate bias VBB2 is supplied to the NMOS ***second gate*** 18, while the substrate bias VBB1 is supplied to the PMOS ***second gate*** 19. By the application of the substrate biases, the threshold voltage of the NMOS transistor 11 attains 0.2V, while the. . .

Fig. 19 shows steps for manufacturing the SOI structure shown in Fig. 16. In Fig. 19(a), a ***silicon*** oxide film is formed on the ***silicon*** substrate 15, and thereafter a polysilicon layer as the ***second gates*** 18 and 19 are formed by sputtering or the like.

Then, referring to Fig. 19(b), an oxide film is deposited, and thereafter the ***silicon*** oxide film is ground by a prescribed thickness (to the dotted line in the figure).

Then, referring to Fig. 19(c), the ***silicon*** layer 40 is deposited.

Although ***silicon*** was used for the semiconductor in the embodiments shown in Figs. 1 to 19, other semiconductor material such as germanium. . .

☐ **L21 ANSWER 35 OF 37 EUROPATFULL COPYRIGHT 2004 WILA on STN**

Accession Number

EP474474 EUROPATFULL ED 20000723 EW 199211 FS OS STA B

Title

Semiconductor light valve device and process for fabricating the same.

Abstract

The invention provides a semi-conductor light valve device and a process for fabricating the same. The device comprises an insulating substrate (7) having a semi-conductor single crystal thin film (1) over at least a portion thereof and providing a pixel array region and a peripheral circuit region. The pixel array region includes a plurality of switch elements (2) for selectively energising a plurality of pixel electrodes (3), and the peripheral circuit region includes drive circuits (15, 16) for operating the switch elements. At least circuit elements of the drive circuits are formed from the semi-conductor single crystal thin film.

In the fabricating process, the semi-conductor single crystal thin film and the insulating substrate are formed as a composite substrate by adhering a semiconductor single crystal plate to the surface of the insulating substrate and by polishing the single crystal plate. The circuit elements of the drive circuits are then formed by treating the single crystal plate. <image>

DETDEN. . .

In the case that the switch elements of the pixel array unit in the prior art are miniaturised, their ***breakdown voltage*** also raises a problem. Specifically, the individual pixels and the light valve device of the active matrix device are supplied. . . Therefore, . . . preferred form its to provide a light valve substrate semi-conductor device, in which switch element MOSFETs having a specially high ***breakdown voltage*** are finely integrated with a high density.

. . .

pixel array region. In figure 14, only the boundary of these two regions is partially shown. In this example, the ***silicon*** single crystal thin film existing in the pixel array region is etched off all over the surface to expose the. . . 104, which is patterned to a pre-determined shape, to form a plurality of island element regions 105 made of the ***silicon*** single crystal thin film 103. For simple illustrations, only one element region is shown in figure 14.

At a step shown in figure 15, the surface and side of the ***silicon*** single crystal thin film 103 patterned into the island shapes are subjected to a thermal oxidation to form a gate insulating film 106 made of ***silicon*** dioxide.

At a step shown in figure 16, a polycrystal ***silicon*** film is deposited by the chemical vapour deposition process to cover all over the surface of the substrate 101. This polycrystal ***silicon*** film is selectively etched by means of a resist mask (although not shown), which is patterned into a pre-determined shape, to form a ***first gate*** electrode G1 on the surface of the gate insulating film 106. Simultaneously with this, the polycrystal ***silicon*** film is selectively etched in the pixel array region, too, to form a ***second gate*** electrode G2.

☐ **L20 ANSWER 1 OF 2 SCISEARCH COPYRIGHT (c) 2004 The Thomson Corporation. on**

Accession Number

93:16105 SCISEARCH

GA The Genuine Article (R) Number: KE569

Title

2-DIMENSIONAL DEVICE SIMULATION OF 0.1-MU THIN-FILM SOI MOSFETS

Author/Inventor

JOACHIM H O; YAMAGUCHI Y; ISHIKAWA K; KOTANI N; NISHIMURA T; TSUKAMOTO K

Source

IEICE TRANSACTIONS ON ELECTRONICS, (**DEC 1992**) Vol. E75C, No. 12, pp. 1498-1505. ISSN: 0916-8524.

Abstract

Thin- and ultra-thin-film SOI MOSFET's are promising candidates to overcome the constraints for future miniaturized devices. This paper presents simulation results for a 0.1 mum gate length SOI MOSFET structure using a two-dimensional/two-carrier device simulator with a nonlocal model for the avalanche induced carrier generation. For the suppression of punchthrough effect in devices with a channel doping of 1 x 10(16) cm-3 and 5 nm thick gate oxide it is found that the SOI layer thickness has to be reduced to at least 20 nm. The thickness of the ***buried oxide*** should not be smaller than 50 nm in order to avoid the degradation of thin SOI performance advantages. Investigating ways to suppress the degradation of the subthreshold slope factor at these device dimensions it was found in contrast to the common expectation that the S-factor can be improved by increasing the body doping concentration. This phenomenon, which is a unique feature of thin-film fully depleted SOI MOSFET's, is explained by an analytical model. At lower doping the area of the current flow is reduced by a decreasing effective channel thickness resulting in a slope factor degradation. Other approaches for S-factor improvement are the reduction of the channel edge capacitances by source/drain engineering or the decrease of SOI thickness or gate oxide thickness. For the latter approach a higher permittivity gate insulating material should be used in order to prevent tunnelling. The low ***breakdown voltage*** can be increased by utilizing an LDD structure to be suitable for a 1.5 V power supply. However, this is at the expense of reduced current drive. An alternative could be the supply voltage reduction to 1.0 V for single drain structure use. A ***dual -gated*** SOI MOSFET has an improved performance due to the parallel combination of two MOSFET's in this device. A slightly reduced ***breakdown voltage*** indicates a larger drain electric field present in this structure.

Supplementary Terms

Author Keywords: THIN-FILM SOI MOSFETS; MINIATURIZED DEVICES; DEVICE SIMULATION

☐ **L20 ANSWER 2 OF 2 DISSABS COPYRIGHT (C) 2004 ProQuest Information and**

Accession Number

2003:37891 DISSABS Order Number: AAI3069817

Title

Electrical characterization of silicon-on-insulator wafers

Author/Inventor

Kang, Sunggun [Ph.D.]; Schroder, D. K. [advisor]

Patent Assignee/Corporate Source

Arizona State University (0010)

Source

Dissertation Abstracts International, (**2002**) Vol. 63, No. 11B, p. 5408. Order No.: AAI3069817. 124 pages. ISBN: 0-493-89503-5.

Abstract

Silicon-on-Insulator (SOI) metal oxide semiconductor field effect transistors (MOSFET) have become a common subject in the semiconductor community due to enhanced performance such as simple processing, excellent scalability, sharp subthreshold characteristics, minimum short-channel effects, and reduced hot electron degradation. Since these films are used for devices, it is necessary to know the SOI film quality with simple and nondestructive methods. In this study, surface photovoltage (SPV) measurements, pseudo-MOSFET characterization, and capacitance-voltage (C-V) are used. Literature review and simulations show that material properties of SOI wafers can have significant effects on the device and circuit performance such as floating body effects, switching speed, leakage current, and noise characteristics. SPV results show the surface charges of SOI wafers to increase with frequency in the low frequency region, with several interface components acting in opposing directions. Iron contaminated wafers show increased surface charges due to a high density of interface states. The efficacy of surface passivation is clearly shown by measuring the effective generation lifetime as a function of time after applying the liquid to the pseudo-MOSFET surface. A more controlled method is the additional ***top gate*** controlling either the upper or lower silicon film surface, separately. C-V measurements for some SOI wafers show a leaky ***buried oxide*** (***BOX***) and high density of interface states. SOI wafers can exhibit quite different ***breakdown voltage*** before and after removing the Si layer, indicating that the gate current flows through weaker current paths in the ***BOX*** beyond the gate area. Transmission electron microscopy (TEM) images display smooth interfaces and a clean ***BOX***, regardless of the ***breakdown voltage***.